PATENT **01AB077/ALBRP228US**

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being submitted *via* the USPTO EFS Filing System on the date shown below to Mail Stop Appeal Briefs - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Date: May 27, 2008 /Rebecca Stanford/
Rebecca Stanford

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant(s): Mark Flood, *et al.*

Serial No: 09/862,941

Filing Date: May 22, 2001

Examiner: Kyung H. Shin

Art Unit: 2143

Title: APPARATUS FOR MULTI-CHASSIS CONFIGURABLE TIME SYNCHRONIZATION

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF

Dear Sir:

Appellants' representative submits this brief in connection with an appeal of the above identified application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [ALBRP228US].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Rockwell Technologies, L.L.C., the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

Appellant, appellants' legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))

Claim 2 has been canceled, and claims 1, 3-53 stand rejected by the Examiner. The rejection of claims 1-53 is being appealed.

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

No claim amendments have been filed after the Final Office Action.

V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

A. Independent Claim 1

Independent claim 1 recites a time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising: a processor interface for interfacing the synchronization apparatus with a host processor; a transmitter adapted to transmit synchronization information and data to a network in the control system; a receiver adapted to receive synchronization information and data from the network; and a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. (*See e.g.*, page 9, lines 18-26; page 10, lines 10-36; page 38, lines 24-29; FIGS. 1, 2, 33, 34).

B. Independent Claim 38

Independent claim 38 recites a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising: a host processor in communication with the first controller via a backplane bus in the control chassis; a transmitter adapted to transmit synchronization information and data to a network in the control system; a receiver adapted to receive synchronization information and data from the network; a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor; and a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave. (*See e.g.*, page 9, lines 18-26; page 10, lines 10-36; page 38, lines 9-29; FIGS. 1, 2, 33, 34).

C. Independent Claim 39

Independent claim 39 recites a synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising: a processor interface for interfacing the synchronization circuit with a host processor; a transmitter component adapted to transmit synchronization information and data to a network in the control system; a receiver component adapted to receive synchronization information and data from the network; and a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor, the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (*See e.g.*, page 9, lines 18-26; page 10, lines 10-36; page 38, lines 9-29; FIGS. 1, 2, 33, 34).

C. Independent Claim 52

Independent claim 52 recites a synchronization system for synchronizing a first controller with a second controller in a control system, comprising: means for interfacing the synchronization circuit with a host processor (*see e.g.*, page 9, line 27-page 10, line 26; page 11, line 27-page 12, line 4; page 38, line 9-page 41, line 6; FIGS. 1, 2, 33, 34); means for transmitting synchronization information and data to a network in the control system (*see e.g.*, page 26, line 27-page 32, line 10; FIGS. 1, 2, 10, 11, 33, 34); means for receiving synchronization information and data from the network (*see e.g.*, page 26, line 27-page 32, line 10; FIGS. 1, 2, 10, 11, 33, 34); and means for maintaining an indication of time according to information received from one of the network and the host processor, the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave (*see e.g.*, page 37, lines 6-15; page 39, lines 1-18; FIGS. 1, 2, 10, 11, 33, 34).

D. Dependent Claims 4 and 15

Dependent claims 4 and 15 substantially recite the transmitter of the time synchronization apparatus periodically transmits message frames every 50μs. (*See e.g.*, page 13, ll. 10-16).

E. Dependent Claims 5 and 16

Dependent claims 5 and 16 substantially recite the transmitter of the time synchronization apparatus transmits a message frame having an LCM indicator at a least common multiple (LCM) interval. (*See* page 13, ll. 20-22).

F. Dependent Claims 6 and 17

Dependent claims 6 and 17 substantially recite the LCM interval is 600ms. (*See* page 13, ll. 22-23).

G. Dependent Claim 18

Dependent claim 18 recites the timing system is adjusted according to the LCM indicator. (*See* page 26, line 31 – page 27, line 2).

H. Dependent Claim 19

Dependent claim 19 recites the receiver interrupts the host processor according to the LCM indicator. (*See* page 30, ll. 3-6).

I. Dependent Claim 35

Dependent claim 35 recites the time synchronization apparatus is configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. (*See* page 18, line 14 – page 19, line 4).

J. Dependent Claim 53

Dependent claim 53 recites the synchronization apparatus exists in a different synchronization time zone from that of the host processor. (*See* page 14, ll. 15-26).

VI. Grounds of Rejection to be Reviewed (37 C.F.R. § 41.37(c)(1)(vi))

A. Whether claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 are unpatentable under 35 U.S.C. §103(a) over Yamanaka, *et al.* (US 4,807,259) in view of Voth (US 6,199,169).

B. Whether claims 8-12 are unpatentable under 35 U.S.C. §103(a) over Yamanaka, *et al.* (US 4,807,259) in view of Voth (US 6,199,169) in further view of Ramussen, *et al.* (US 6,449,732).

C. Whether claims 29, 35-37, and 47 are unpatentable under 35 U.S.C. §103(a) over Yamanaka, *et al.* (US 4,807,259) in view of Voth (US 6,199,169)in further view of Kuribayashi, *et al.* (US 6,775,246).

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

A. Rejection of Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 Under 35 U.S.C. §103(a)

Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, *et al.* (US 4,807,259, hereinafter referred to as "Yamanaka") in view of Voth (US 6,199,169). It is respectfully submitted that this rejection should be reversed for at least the following reasons. Neither Yamanaka nor Voth, either alone or when combined, disclose all the claimed features. Moreover, Yamanaka and Voth produce an inoperative combination and/or do not yield a reasonable expectation of success to make the proposed combination. Therefore, these references are not permissibly combinable, and furthermore, the Examiner relies upon mere conclusory statements to uphold these rejections.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***. In addition, ***there must be a reasonable expectation of success to make the proposed combination***. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR v. Teleflex*, 550 U.S. ___, 127 S. Ct. 1727 (2007) *citing In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006).
>
> ***If references taken in combination would produce a "seemingly inoperative device," we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness***. *In re Sponnoble,* 405 F.2d 578, 587, 160 USPQ 237, 244, 56 C.C.P.A. 823 (1969) (references teach away from combination if combination produces seemingly inoperative device); *see also In re Gordon,* 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (inoperable modification teaches away). *McGinley v. Franklin Sports Inc.*, 262 F.3d 1339, 60 USPQ2d 1001, 1010 (Fed. Cir. 2001) (emphasis added).

The claimed subject matter relates generally to industrial control systems (*see, e.g.*, control system 50, FIG. 2) with a time synchronization apparatus (*see, e.g.*, S/L 82, FIG. 2) for

synchronizing operation of a first controller (*see, e.g.*, controller 56, FIG. 2) with that of a second controller (*see, e.g.*, controller 54, FIG. 2). More specifically, the time synchronization apparatus can be configured to operate as either a master or a slave (and therefore a single apparatus can be configurable as both), can synchronize across disparate and/or multiple time synchronization zones (*see e.g.*, pg. 12, line 15 – pg. 14, line 26) and can function in topologies other than a star topology such as a daisy chain or loop configuration, or combinations thereof (*see e.g.*, pg. 18, ll. 15-17). In particular, independent claim 1 recites, "a processor interface for interfacing the synchronization apparatus with a host processor, the time synchronization apparatus is ***configurable*** *to operate* ***as both*** *a synchronization master and a synchronization slave*." Likewise, independent claim 38 (and similarly claims 39 and 52) recites, "a synchronization circuit…*configurable* ***by the host***." Yamanaka does not disclose such features.

Yamanaka relates to a time synchronization method, wherein the time of a slave clock is synchronized with the time of a master clock. (*See* col. 7, ll. 6-49). The master clock resides in a master station (*see* element 17, FIG. 3A) and the slave clock resides in a slave station (*see* element 37, FIG. 3B) that are structurally designed to be physically specific and distinct. *Inter alia*, a master station needs at least twice as many registers as a slave station if synchronizing serially, and at least a factor of $(n + 1)$ times as many registers, where n is the number of slave stations to be synchronized, when operating in parallel. (*See e.g.*, col. 7, ll. 26-30). While Yamanaka discloses synchronizing a slave clock, the reference is silent as to whether these stations are configurable. Moreover, given distinctions included in the necessary hardware structure between a master station and a slave station, configurability is not contemplated, and in fact the reference therefore teaches away from configurability. References that teach away cannot serve to create a prima facie case of obviousness. *In re Gurley,* 27 F.3d 551, 553, 31 USPQ2d 1130 (Fed. Cir. 1994). Accordingly, Yamanaka does not teach a time synchronization apparatus that is ***configurable to operate as both a synchronization master and a synchronization slave***. Moreover, with regard to at least independent claims 38, 39, and 52, Yamanaka further does not teach or suggest a synchronization circuit…*configurable* ***by the host***.

At page 2 of the Advisory Action (dated March 19, 2008), the Examiner concedes these deficiencies with respect to Yamanaka, but argues that Voth, which teaches a software-based "synchronization" system (*see* Voth Abstract) that utilizes UNIX operating system calls to "synchronize" slave nodes (*see* Voth col. 4, ll. 14-16), discloses configurable nodes. The

Examiner does not provide analysis regarding the Yamanaka's teachings away from configurability. Rather, at page 10 of the Final Office Action (dated December 27, 2008) it is simply argued that it would have been obvious to combine these references "in order to enable the capability to network communications over a wide range of network configurations and topologies." Appellants respectfully submit there are a number of errors extant in this analysis.

Foremost, in the Decision on Appeal (mailed February 9, 2007), the BPAI reversed all rejections set forth by the Examiner as Voth is materially deficient to disclose the synchronization apparatus of the subject claims. Accordingly, Voth at most teaches configurability of something that is decidedly not the claimed synchronization apparatus, while, neither reference teaches a "***time synchronization apparatus*** that is ***configurable***…." Therefore, the Examiner's analysis rests squarely on the proposition that the stations of Yamanaka are to be combined with the *concept* of configurability purportedly disclosed by Voth. However, Yamanaka teaches away from configurability (given different physical hardware structure between master stations and slave stations). Regardless, Voth does not expressly disclose that nodes are configurable, yet this feature has been merely assumed in the analysis to exist. In addition, Voth is also silent as to whether the nodes are configurable ***by the host*** as recited in independent claims 38, 39, and 52. Second, reconfiguring a slave to operate as a master with respect to software system calls is materially distinct from causing such changes to affect existing hardware, as would be required if Yamanaka were to reconfigure a slave to a master. For example, in Voth a slave node might only be required to send rather than receive SYNC messages, whereas in Yamanaka, the slave station would need structural additions to its circuitry. Accordingly, even if Voth is deemed to teach the concept of configurable nodes, one of ordinary skill in the art would not be motivated to look to Voth and there is no indication that the teachings of Voth would impart a reasonable expectation of success when applied to Yamanaka.

Third, a combination of Voth with Yamanaka would produce a seemingly inoperative device for at least the following reasons. As discussed, Voth is software-based and is actually not true synchronization (discussed *infra*). Voth employs a "trick" to simulate synchronization that becomes possible in very narrow situations, such as in SSI clusters (*see* Voth col. 2, ll. 55-56) with a very high speed TNet (*see* Voth col. 4, ll. 19-21). Such conditions do not exist in the data transmission system of Yamanaka. Moreover, Voth is expressly designed to function in "networks where ethernet simplification does not apply" (*see* Voth col. 2, ll. 29-30), wherein

ethernet simplification is defined as using round-trip travel times between nodes and dividing by two to calculate the propagation delay (*see* Voth col. 1, line 59 – col. 2, line 9). Pointedly, what is described here as ethernet simplification is precisely what is relied upon by Yamanaka (*see* Yamanaka equation at col. 7, line 32, where propagation delay, τ_1, is calculated as the round-trip travel time with an offset, divided by 2). Hence, Voth itself distinguishes from Yamanaka, noting that Yamanaka is ineffective in systems for which Voth is designed to fit and it can further be shown that Voth is inoperable in systems for which Yamanaka is applied.

The method for time synchronization disclosed in Voth relies upon the assumption that the round-trip time (transmission delay or latency) between master and slave is zero. (*See* Voth col. 6, ll. 60-63, where the method performs a round-trip, from the master to the slave and back to the master, then calculates the difference between the time stamps of the master and the slave ***with no offset for the travel time*** of the SYNC message between the two nodes). Although Voth probably understands that instantaneous propagation of the SYNC message is of course impossible, the assumption that the round-trip travel is zero is not necessarily invalid due to the fact that no time difference between clocks is detectable if that difference is less than 1 clock tick. (*See* Voth col. 8, ll. 60-63). Thus, Voth does not care what the actual round-trip time is for the SYNC message *as long as the round-trip travel time is less than half of one clock tick*, because in that case, the clocks will have the *appearance* of being synchronized. (*See* Voth col. 8, ll. 64-67).

Hence, the accuracy of the method disclosed in Voth is a function of the speed of the network *versus* the clock frequency of the nodes (*see e.g.*, Voth col. 8, ll. 57-60), and while the round-trip time is assumed to be zero in the synchronization calculation, the ***maximum*** round-trip time ***must be less than half of 1 tick***, or the SYNC message will be rejected terminating the method. (*See* Voth col. 6, ll. 50-53). Thus, the time value of ½ of a tick or clock cycle functions as an upper limit on the accuracy of Voth. (*See* Voth col. 8, ll. 46-49). Therefore, Voth is suitable for SSI computer clusters as disclosed, but is wholly inapplicable to data transmission system networks such as that of Yamanaka or the control system of the subject claims. In contrast, Yamanaka calculates the transmission delay, τ_1, (by averaging the round-trip times) in order to perform synchronization (*see* Yamanaka col. 7, line 32), whereas the "trick" of Voth is to assume this value is zero, but below an upper limit defined by the clock frequency of the master node processor. Accordingly, the combination of Yamanaka and Voth would produce a

seemingly inoperative device, which cannot therefore stand as predicates for a *prima facie* case for obviousness.

The Examiner does not appear to fully consider the above rationale, but at page 3 of the Final Office Action, the Examiner relies upon the assumption that technological advances, especially in network speeds can allow Voth to apply to control systems of the subject claims, and also to different time zones by applying Voth to the Internet at large (*see* page 5). However, both of these arguments are erroneous, as they would require a repeal of accepted laws of nature. To illustrate such and to provide further support for the fact that there is no reasonable expectation of success to combine Voth with Yamanaka, consider the following example:

Today, current processors run at a clock frequency of about 1000 MHz, or about 1 billion ticks per second. It is further known based upon currently accepted physics principles that information cannot be transmitted faster than the speed of light (*e.g.*, 300 million meters per second). Therefore, it can be stated that light will travel about $10^9/3^8 = 3.33$ meters per clock cycle (or tick) or 1.67 meters for every ½ tick. Applying the method of Voth, and assuming the SYNC message can travel no faster than the speed of light, then the round-trip travel distance between 2 nodes must be no greater than 1.67 meters. And since this is a round-trip, the nodes must actually be no greater than 0.835 meters apart, or Voth is guaranteed to exceed the maximum round-trip time, even without any form of network delay and all messages traveling in a straight line at the speed of light. Therefore, even if the synchronization principles recited in Voth and Yamanaka were not mutually exclusive, this example illustrates that Voth cannot be applied to industrial control systems, to systems with different "time zones," to systems that are not a star topology, or to the Internet at large, where nodes could potentially be separated by more than 20 million meters. Thus, quite apart from the Examiner's argument that technological advances can expand the applicability of Voth, such advances have actually rendered the method obsolete, perhaps even in the narrow field of endeavor to which Voth originally applied. Hence, the combination of Yamanaka and Voth does not have a reasonable expectation of success and/or would produce a seemingly inoperative device. Accordingly, the Examiner has failed to present a *prima facie* case for obviousness and this rejection should be reversed.

Still further yet, pursuant to KSR *supra*, the Examiner has not provided some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Rather, the Examiner argues at page 10 of the Final Office action that one of ordinary skill in the

art would have been motivated to employ the teachings of Voth [in combination with Yamanaka] in order to enable the capability to network communications over a wide range of network configurations and topologies. This is a mere conclusory statement not supported, and in fact expressly rejected by Voth. For example, the Examiner points to column 2, lines 27-30 to stand for the proposition that Voth can be applied to the Internet at large, when in fact that very portion (along with the comments *supra*) indicates Voth cannot be used with the Internet at large (*e.g.*, utilizing ethernet simplification). Accordingly, the combination of Voth with Yamanaka cannot provide any additional capability or additional network configurations or topologies. Rather, Voth can only serve to limit or change (in a mutually exclusive manner) the types of networks and topologies for which Yamanaka could apply, even if the combination were not inoperable. Accordingly, this rejection should be reversed for yet another reason

Claims 4-6 and 15-19

Claims 4 and 15 recite a transmitter that periodically transits message frames at a fixed period of 50μs. Voth clearly does not teach this limitation. Rather, Voth merely indicates that messages can be transmitted at fixed intervals, and expressly teaches an update cycle of 20 seconds (*see* col. 9, ll. 20-21), and further teaches that the update cycle *takes about 4 seconds to complete* (*see* col. 8, ll. 21-22). However, at page 2 of the Advisory Action, the Examiner argues that 50μs is a fixed interval taught by Voth. Yet, while Voth discloses that that messages can be transmitted at fixed intervals, the reference is limited to fixed intervals of at least 4 seconds or greater, and more specifically, certainly does not teach or suggest a fixed interval of about 50μs. Appellants note that even were it possible for Voth to use a 50μs update cycle (rather than the expressly taught 20 seconds), this would mean that Voth would try to update each node about 80,000 times in the 4 seconds it takes to complete a single update, in essence spending 80,000 times the resources it costs to do a job once, each and every time and for each and every node. Such a situation defies reason and would be so wasteful of processor and network resources that a single node probably could not ever be properly synchronized, much less a system with many nodes. Accordingly, it is not germane to suggest that Voth teaches a specific fixed interval of 50μs, and this rejection with respect to clams 4 and 15 should be reversed.

Similarly, claims 6, and 17 recite a transmitter transmits a message frame having an LCM indicator at a least common multiple of 600ms. It is readily apparent that Voth does not teach

600ms, for at least the reasons provided above with respect to claims 4 and 15. Moreover, regarding claims 5 and 16 (*et al.*), Voth cannot even have an LCM (least common multiple) interval at for at least two reasons: 1) Voth assumes latency between nodes is zero, and therefore all nodes would have a latency of zero, so there is no LCM; 2) Voth only contemplates a star configuration, where all nodes are connected to the master. The Final Office Action argues at pages 11-12 that the update cycle of Voth is equivalent to the LCM of the claim, however, the Examiner previously argued that Voth's update cycle was the fixed period of claim 4. Clearly, Voth's update cycle cannot simultaneously represent disparate features of the claims. Hence, regarding at least claims 5, 6, 16-19, this rejection should be reversed.

Claim 53

Neither Voth nor Yamanaka teach the synchronization apparatus exists in a different synchronization time zone or coordinate system time from that of the host processor as recited in dependent claim 53. At pages 28-29 of the Final Office Action, the Examiner argues to the contrary citing Voth at column 4, lines 17-19 and suggesting that "distributed internetworking environment such as the Internet operates across time zones." Be that as it may, such a statement has nothing whatever to do with Voth. Neither at the indicated portions nor anywhere else does Voth teach these features. Rather, Voth is expressly indicated to operate in a high speed TNet, which is not the Internet. Voth cannot function if the network were the Internet due to a latency that would render the method of Voth worthless, as any latency that is greater than half a clock cycles makes Voth inoperable. (*See* Voth col. 8, ll. 60-66). The Internet spans the entire globe, yet even at the speed of light (much less the fastest networks known today), Voth's method of time synchronization would be incapable of functioning at inter-node distances greater than about 0.835 meters. Accordingly, the Examiner's rationale is precluded by well-known natural limits, and this rejection as to claim 53 should be reversed

B. <u>Rejection of Claims 8-12 Under 35 U.S.C. §103(a)</u>

Claims 8-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, in view of Voth and Ramussen, *et al.* (US 6,449,732, hereinafter referred to as "Ramussen"). Withdrawal of the rejection is respectfully requested because Yamanaka, Voth,

and Ramussen, *et al.*, either alone or in combination with one another, do not teach all the claimed features.

In particular, claims 8-12 depend directly or indirectly upon independent claim 1. As noted *supra*, the cited references do not teach or suggest each and every feature recited in the subject claims. Ramussen, *et al.* fails to make up for the aforementioned deficiencies of Yamanaka and Voth with respect to independent claim 1. Thus, this rejection with respect to claims 8-12 should be reversed for at least the reasons commented on *supra* in §A.

C. Rejection of Claims 29, 35-37 and 47 Under 35 U.S.C. §103(a)

Claims 29, 35-37, and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka in view of Voth and in further view of Kuribayashi, *et al.* (US. 6,775,246, hereinafter referred to as "Kuribayashi"). Withdrawal of the rejection is respectfully requested for at least the following reasons. Yamanaka, Voth, and Kuribayashi all fail to teach the all features of the claims, either alone or in combination with one another.

Claims 29, 35-37 depend directly or indirectly from independent claim 1 while claim 47 depends directly or indirectly from independent claim 39. As noted *supra*, the combination of Yamanaka and Voth fails to teach or suggest all aspects of the subject claims. Kuribayashi fails to make up for the aforementioned deficiencies with respect to independent claims 1 and 39. Thus, this rejection should be reversed.

In addition, independent claim 35 recites, the time synchronization apparatus of claim 1, being configured as an intermediate node in a ***daisy-chain topology***, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. Neither Voth nor Kuribayashi, *et al.* teach or suggest a daisy-chain topology. The examiner alleges that Kuribayashi, *et al.* teaches a daisy-chain topology, yet neither the indicated portions nor anywhere else does the reference teach this aspect. Moreover, the method disclosed in Voth relies on direct and nearly instantaneous communication between the nodes in order to affect time synchronization because the method treats the round-trip time of communication between the nodes as zero. Therefore, even if Kuribayashi, *et al.* did teach a daisy-chain topology, the combination of a daisy-chain topology from Kuribayashi, *et al.* would render the time synchronization method disclosed in Voth inoperable because at least one clock cycle

would be required to assert an instruction to forward the SYNC message to another node (and more clock cycles for each node connected along the daisy-chain), thereby effectively guaranteeing that all round-trip times will exceed the maximum allowable value (*i.e.*, one-half of a clock cycle) and be rejected, terminating the method without any synchronization occurring. (*See* Voth col. 6, ll. 50-55).

D. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-53 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP228US].

Respectfully submitted,

AMIN & TUROCY, LLP

/Himanshu S. Amin/
Himanshu S. Amin
Reg. No. 40,894

AMIN & TUROCY, LLP
24TH Floor, National City Center
1900 E. 9TH Street
Cleveland, Ohio 44114
Telephone (216) 696-8730
Facsimile (216) 696-8731

VIII. Claims Appendix (37 C.F.R. § 41.37(c)(1)(viii))

1. A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:

a processor interface for interfacing the synchronization apparatus with a host processor, the time synchronization apparatus is configurable to operate as both a synchronization master and a synchronization slave;

a transmitter adapted to transmit synchronization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network; and

a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor.

2. (Canceled).

3. The time synchronization apparatus of claim 1, being configured to operate as a synchronization master, the transmitter periodically transmits message frames at a fixed period, the synchronization apparatus is a hardware module coupled to the host processor.

4. The time synchronization apparatus of claim 3, the fixed period is about 50μs.

5. The time synchronization apparatus of claim 3, the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval.

6. The time synchronization apparatus of claim 5, the LCM interval is 600ms.

7. The time synchronization apparatus of claim 3, being configured as a synchronization master, the transmitter transmits message frames having multiplexed data and direct data.

8. The time synchronization apparatus of claim 7, the frame comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes.

9. The time synchronization apparatus of claim 8, the data field comprises 6 32 bit words, and the amount of multiplexed data and the amount of direct data in each message frame is configurable.

10. The time synchronization apparatus of claim 9, each message frame comprises a direct data portion and a multiplexed data portion, the direct data comprises the direct data portion of a single frame, and the multiplexed data comprises the multiplexed data portions of a plurality of frames.

11. The time synchronization apparatus of claim 10, the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame.

12. The time synchronization apparatus of claim 9, the amount of multiplexed data and the amount of direct data in each message frame is configurable according to information from the host processor.

13. The time synchronization apparatus of claim 7, the timing system is adjustable according to information received from the host processor.

14. The time synchronization apparatus of claim 1, being configured as a synchronization slave, the receiver receives message frames at a fixed period, and the timing system is adjusted according to the fixed period.

15. The time synchronization apparatus of claim 14, the fixed period is about 50μs.

16. The time synchronization apparatus of claim 14, the receiver receives a message frame having an LCM indicator at a least common multiple (LCM) interval.

17. The time synchronization apparatus of claim 16, the LCM interval is 600ms.

18. The time synchronization apparatus of claim 16, the timing system is adjusted according to the LCM indicator.

19. The time synchronization apparatus of claim 16, the receiver interrupts the host processor according to the LCM indicator.

20. The time synchronization apparatus of claim 14, the transmitter transmits message frames at the fixed period.

21. The time synchronization apparatus of claim 20, the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data.

22. The time synchronization apparatus of claim 21, the message frames comprise a data field with 6 32 bit words, and the amount of multiplexed data and the amount of direct data in each message frame is configurable.

23. The time synchronization apparatus of claim 22, each message frame comprises a direct data portion and a multiplexed data portion, the direct data comprises the direct data portion of a single frame, and the multiplexed data comprises the multiplexed data portions of a plurality of frames.

24. The time synchronization apparatus of claim 23, the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame.

25. The time synchronization apparatus of claim 24, the receiver presents direct data from received message frames to the host processor at the fixed period.

26. The time synchronization apparatus of claim 25, the receiver presents multiplexed data from received message frames to the host processor at a multiple of the fixed period.

27. The time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value from the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, the multiplication result value is the product of the multiplication value and the operand.

28. The time synchronization apparatus of claim 27, the direct data received in the message frame comprises the operand.

29. The time synchronization apparatus of claim 14, the message frame comprises a status component indicative of the status of an upstream device, the receiver provides the status component to the host processor.

30. The time synchronization apparatus of claim 14, the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data.

31. The time synchronization apparatus of claim 30, at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, the direct data from a received message frame is passed through to the transmitter.

32. The time synchronization apparatus of claim 30, comprising a multiplier, at least a portion of the direct data in the message frames transmitted by the transmitter comprises a multiplication result value provided to the transmitter by the multiplier.

33. The time synchronization apparatus of claim 30, at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor.

34. The time synchronization apparatus of claim 33, the multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor.

35. The time synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain.

36. The time synchronization apparatus of claim 35, the receiver receives message frames at a fixed period, and the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data.

37 The time synchronization apparatus of claim 36, at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, the direct data from a received message frame is passed through to the transmitter.

38. A synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

a host processor in communication with the first controller via a backplane bus in the control chassis;

a transmitter adapted to transmit synchronization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network;

a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor; and

a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave.

39. A synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising:

a processor interface for interfacing the synchronization circuit with a host processor;

a transmitter component adapted to transmit synchronization information and data to a network in the control system;

a receiver component adapted to receive synchronization information and data from the network; and

a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor,

the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave.

40. The system of claim 39, the transmitter component periodically transmits message frames comprising direct data, and the direct data is obtained from at least one of the receiver component and the host processor.

41. The system of claim 39, further comprising a multiplier, the transmitter component periodically transmits message frames comprising direct data, and the direct data is obtained from at least one of the receiver, the host processor, and the multiplier.

42. The system of claim 39, the transmitter component periodically transmits message frames comprising multiplexed data, and the multiplexed data is obtained from the host processor.

43. The system of claim 39, the transmitter component periodically transmits message frames comprising direct data and multiplexed data, and the amount of the multiplexed data in the message frames and the amount of direct data in the message frames is configurable.

44. The system of claim 39, the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and the synchronization circuit provides at least one of received direct data, received multiplexed data, and received status information from the receiver component to the host processor.

45. The system of claim 44, further comprising a multiplier operating on the received direct data, and the synchronization circuit provides a multiplier result value from the multiplier to the host processor.

46. The system of claim 45, the synchronization circuit provides a multiplication value to the multiplier from the host processor.

47. The system of claim 44, the status information comprises at least one of status of an upstream device, and an error counter.

48. The system of claim 39, the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and the synchronization circuit provides at least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor.

49. The system of claim 39, the transmitter component periodically transmits message frames having synchronization information, the synchronization information is obtained from the timing system, and the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor.

50. The system of claim 39, the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver.

51. The system of claim 39, the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor.

52. A synchronization system for synchronizing a first controller with a second controller in a control system, comprising:

means for interfacing the synchronization circuit with a host processor;

means for transmitting synchronization information and data to a network in the control system;

means for receiving synchronization information and data from the network; and

means for maintaining an indication of time according to information received from one of the network and the host processor, the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave.

53. The time synchronization apparatus of claim 1, the synchronization apparatus exists in a different synchronization time zone from that of the host processor.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.